Attachment A

1.   (Cancelled)

2.   (Currently amended) The ~~method~~ computing system as recited in claim ~~1~~ 18 wherein each receiving node sends an acknowledge to a respective sending node at a predetermined time with respect to sending a corresponding packet, to indicate successful delivery of the corresponding packet to the sending node, thereby providing a fixed time for the sending node to know whether a packet was successfully transmitted.

3.   (Currently amended) The ~~method~~ computing system as recited in claim 2 wherein the sending node determines that transmission of a packet was unsuccessful by checking if the acknowledge was returned after the predetermined time has elapsed.

4.   (Currently amended) The ~~method~~ computing system as recited in claim 3 wherein the receiving node sends a no acknowledge (nack) at the predetermined time to the sending node on detection of an error condition in receipt of the packet.

5.   (Currently amended) The ~~method~~ computing system as recited in claim 4 wherein the error condition detected by the receiving node is one of a buffer overflow and a checksum error.

6.   (Currently amended) The ~~method~~ computing system as recited in claim 2 wherein unsuccessful transmission is determined by a timeout indicating that an acknowledge failed to arrive after the predetermined time has elapsed.

7.   (Cancelled)

8.   (Currently amended) The ~~method~~ computing system as recited in claim ~~7~~ 18 wherein ~~the~~ requests for transmission paths are contained within the packets sent into at least one

of the low latency switched network and the second switched network and extracted after entry into ~~the~~ a corresponding one of the first and second switch.

9.   (Cancelled)

10.   (Cancelled)

11.   (Currently amended) The ~~method~~ computing system as recited in claim ~~7~~ 18, wherein no buffer space is allocated in a receiving node before a packet is sent from a respective sending node, thereby simplifying switch overhead.

12.   (Currently amended) The ~~method~~ computing system as recited in claim 11 wherein if the receiving node detects a buffer overflow, the receiving node sends a no acknowledge packet (nack) to the sending node indicating that a packet associated with the buffer overflow was not successfully received.

13.   (Cancelled)

14.   (Cancelled)

15.   (Cancelled)

16.   (Cancelled).

17.   (Cancelled)

18.   (Currently amended) A computing system comprising:
a plurality of sending and receiving nodes;
a low latency switched network including a first switch, the first switch being a buffer-less switch coupling the plurality of sending and receiving nodes, the buffer-less switch having a fixed forwarding delay for all packets sent from one of the sending nodes and successfully received by one of the receiving nodes;

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a second switched network, including a second switch coupled to the plurality of sending
and receiving nodes; and

wherein <u>at least one of the plurality of sending and receiving nodes comprises a storage
device and</u> the first switch carries scheduling information for a <u>the</u> storage device
and the second switch carries bulk traffic for at least one of storage and retrieval
on the storage device.

19.   (Cancelled)

20.   (Cancelled)

21.   (Original) The computing system as recited in claim 18 wherein each sending
node includes a send register written into by a sending node to send data across the network.

22.   (Original) The computing system as recited in claim 21 wherein each sending
node includes a status register indicating whether a transfer across the network completed
successfully.

23.   (Original) The computing system as recited in claim 22 wherein the status register
includes a field indicating a type of failure.

24.   (Original) The computing system as recited in claim 22 wherein a sending node
rewrites data into the send register if a transfer across the network for the data completed
unsuccessfully.

25.   (Original) The computing system as recited in claim 18 wherein the buffer-less
switch further comprises:
a plurality of input registers coupled to respective input ports;
switch control logic, coupled to the input registers and responsive to packet information
stored in the registers, to allocate output ports on the switch according to the
packet information;

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and wherein the switch control logic is responsive to allocate output ports on a first come first served basis.

26.   (Original) The computing system as recited in claim 25 wherein respective packet information provided to the switch control logic constitutes respective requests for output ports, and if a first and second request for an output port path collide by requesting the output port at the same time, the switch control logic responds by selecting one of the requests as a winner and dropping a packet associated with the second request.

27.   (Original) The computing system as recited in claim 25 further comprising output registers in the buffer-less switch coupled to receive data selected by respective selector circuits selectively coupled to respective ones of the input ports.

28.   (Original) The computing system as recited in claim 26 wherein the switch control logic selects the winner according to at least one of a random basis and a round robin basis.

29.   (Original) The computing system as recited in claim 18 wherein the low latency switched network includes a plurality of cascaded buffer-less switches, thereby forming a multi-stage buffer-less switch.

30.   (Cancelled)